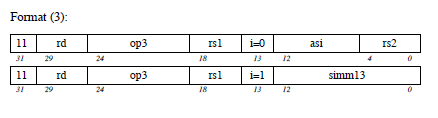
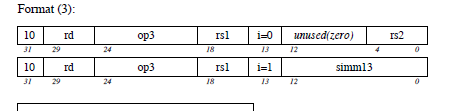
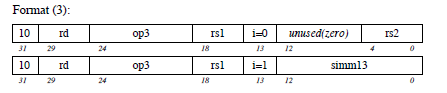
Ld op3 000000



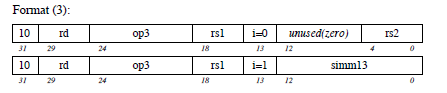
Add op3 000000



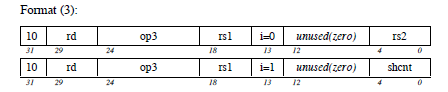
AND op3 010001



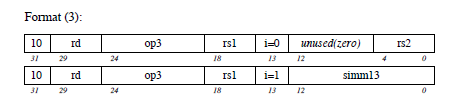
XOR op3 000111



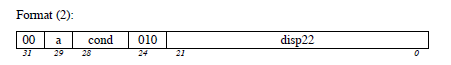
SRL op3 100110



Cmp = subcc op3 010100



BL cond=0011



LEGENDA:

Rd – reg destino. 5bits com address dele

Rs1 – reg operando. 5bitd com address dele

Rs2 - reg operando. 5bitd com address dele

Simm13 – imediato de 13bits; pode ser extendido para até 32 bits

i – i=0, operando é rs2; i=1, operando é simm13 ou shcnt

asi – para load/save alternae instrucion

shcnt – valor a ser deslocado

disp22 – 22bits para word-aligned, sign-extended, PC-relative

displacements em uma branch